UEFI Firmware Solutions for Enterprise Servers: A Case Study in 8-way Processor Support

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Jeff Bobzin - Senior Director Software Architecture, Insyde Software, and Secretary UEFI Board

EFIS005
Agenda

- UEFI promotes scalability - Intel
- 8SG Server Introduction - Inspur
- Firmware for 8-way Server - Insyde
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• UEFI: Unified Extensible Firmware Interface
  – a new model for the interface between the OS and platform firmware
• PI: Platform Initialization
  – Standardization: key to interoperability across implementations
  – Modular components like silicon drivers (e.g. PCI) and value-add drivers (security)
  – Preferred way to build UEFI

UEFI is Architected for Dynamic Modularity
UEFI Pre-boot Advantages

• More robust boot loader using UEFI
  – Easier to implement “Failover Boot” solution
• UEFI Shell: Full featured utility shell
• Easily reload, unload & update UEFI drivers in Pre-OS
• Pre-OS networking - Full IPv4 and IPv6 network stack, PXE boot, iSCSI
• Pre-OS applications can run in UEFI Boot Services layer
  – lot of useful DOS-like tools can be ported to UEFI applications
UEFI Advantages in Scalability

• Defines standard interfaces across different platforms & architectures
• Common code for IA32, X64, and Intel® Itanium® architecture
  – We use the same Intel® 5520 Chipset with 82801JB I/O Controller Hub (ICH10) chipset code across all the segments
• Based on protocols instead of proprietary implementations

UEFI makes scalable server support easier
Intel® QuickPath Interconnect vs. FSB

Intel® QuickPath Interconnect (Intel® QPI) drives a leap forward in Platform Technology

- **Scalable solution**
  - Much higher link bandwidth than FSB
    - Headroom for higher transfer rates
  - Vastly greater MP system bandwidth with multiple, independent memory controllers and Intel QuickPath Interconnect links
    - Scales efficiently with number of processors
  - Many system topologies with more than four processors supported
  - Common interface for Intel® Itanium® and Xeon® Processor based systems

- **Improved system robustness**
  - Additional levels of error recovery and logging for mission critical systems
  - RAS features

Highly Configurable System Interconnect
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Inspur 8SG Server Introduction

- Inspur 8SG Server Overview
- Inspur 8SG Platform Topology
- Inspur 8SG Flexible Partitioning
- Inspur 8SG Advanced RAS Features
- Inspur 8SG Server Management

First 8-socket 8-core modular server in China

Up to 128 logical processors offering exceptional performance!
Inspur 8SG Server Overview

- 8-socket Intel® Xeon® Processor 7500 series (Nehalem-EX), with 64C/128T in 6U mainframe
- 64 DIMMs, up to 1TB size; 204.8GB (25.6GB*8) Memory bandwidth
- Exceptional I/O performance: 72X PCI Express* Gen2
- Advanced RAS features: Intel® Scalable Memory Interconnect (Intel® SMI)/Intel® QPI self healing, Machine Check Architecture, Memory migration, Physical partitioning
Inspur 8-Socket Glueless Platform Topology

- Built upon a 2-socket per IOH building block offering Flexibility and Modularity
- Topology selected to minimized transaction hops and latency
- Single partition includes one legacy IOH, 2 non-Legacy IOHs and one active 82801JB I/O Controller Hub (ICH10)
- 6.4 GT/s link speed is critical to 8-socket glueless performance

UEFI Platform Initialization Specification makes the scalable server support easier
**Inspur 8SG Flexible Partitioning**

- **Flexible system configuration**
  - 8SG system
    - 8SG+3 IOHs+1 ICH
  - 4SG system
    - 4SG+2 IOHs+1 ICH
    - 4SG+1 IOH+1 ICH

- **Intelligent Partitioning**
  - Auto switch front-side device ports
  - Software configure without hardware alteration
  - Enhanced BIOS Design
    - Single BIOS image used for different configurations
  - Enhanced Partition Manage Feature
    - Auto swap between 8S mode and dual 4S mode
## Inspur 8SG Server Advanced RAS Features

<table>
<thead>
<tr>
<th>RAS Features</th>
<th>Types</th>
<th>Descriptions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Memory</strong></td>
<td>Memory Mirroring</td>
<td>Intra socket, Inter socket</td>
</tr>
<tr>
<td></td>
<td>Memory Demand and Patrol scrubbing</td>
<td>Demand scrubbing: write corrected data back to the memory once a correctable error is detected on a read transaction. Patrol scrubbing: proactively searches the system memory, repairing correctable errors.</td>
</tr>
<tr>
<td></td>
<td>DRAM SDDC</td>
<td>x4 or x8 Single Device Data Correction</td>
</tr>
<tr>
<td><strong>System Link Layer</strong></td>
<td>Self-healing</td>
<td>Downshift link width on the error link</td>
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<td></td>
<td>Lane Failover</td>
<td>Adaptive routing</td>
</tr>
<tr>
<td></td>
<td>CRC</td>
<td>Cyclic redundancy check</td>
</tr>
<tr>
<td></td>
<td>Clock Failover</td>
<td>Redirect forwarded clocks to the clock fail-over lane</td>
</tr>
<tr>
<td></td>
<td>Link Retry</td>
<td>Restart a cycle on the failure link</td>
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<tr>
<td><strong>System Partitioning</strong></td>
<td>Static hard partitioning</td>
<td>Allows a system to be divided into 2 machines, each capable of running separated OS and applications</td>
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<tr>
<td></td>
<td>Partition via Virtualization</td>
<td>Support for Virtualization features VT-x2/VT-d2</td>
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<tr>
<td><strong>Hot-Plug</strong></td>
<td>Processor Board hot-plug</td>
<td>Dynamic hot-add/remove processor modules</td>
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<tr>
<td></td>
<td>IOH Board hot-plug</td>
<td>Dynamic hot-add/remove IOH modules</td>
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<tr>
<td></td>
<td>PCIe hot-plug</td>
<td>Native PCIe hot-plug support</td>
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</table>
Inspur 8SG Server Management

- **System Management**
  - Intelligent Power Management
  - System Static Partitioning
  - IP KVM Remote Control
  - Virtual Storage Media
  - PCI-E hot-plug support

- **Human-Machine Interface**
  - Colorful LCD touch pad for end user

- **System Status Monitoring and Error Handling**
  - Chip level Error monitoring and handling
  - System thermal event monitoring and handling
  - System Boot-up Monitoring and Management
  - General states monitoring
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Scaling Firmware Solution to 8-way

• Insyde’s challenge: scale up proven 2/4 socket firmware to support 8-way system

• Intel® QuickPath Interconnect link allows system hardware to scale up from proven 2 or 4 socket design to 8-way

• Similarly, modularity of UEFI allows firmware to scale up to meet the challenge of the larger (8-way) system
Project Goals

• Tight schedule: needed to have 8-way hardware running before February Spring Festival

• Schedule goals could only be achieved if firmware project used best techniques
  
1. Analyze the Technical Challenges
2. Break up required development into pieces that could be pre-tested
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1. Analyze the Technical Challenges
2. Break up development into pieces that could be pre-tested
Challenge: Dissect the CPU

The Intel® Xeon® Processor 7500 series has a complex Internal Structure
### Challenge: Processor Initialization

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<tbody>
<tr>
<td><strong>Boot Mode?</strong></td>
<td>Designer chose to use Intel® QPI boot mode – cores will boot from ICH Flash</td>
</tr>
<tr>
<td><strong>Core Count?</strong></td>
<td>Expand tables for 8 (sockets) x 8 (cores) x 2 (threads) == 128</td>
</tr>
<tr>
<td><strong>APIC ID?</strong></td>
<td>3 bits socket ID 5 bits thread ID == 256 IDs Work -- Expand tables</td>
</tr>
<tr>
<td><strong>x2APIC?</strong></td>
<td>Available, must be supported, but APIC still available too. (this is largest server that fits in APIC)</td>
</tr>
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</table>
Challenge: 8 Socket Routing

- This design is ‘Glueless’ → No Node Controller
- Intel® QPI fabric expanded to include 8 Processor sockets
- Processor-to-processor links are 1-hop or 2-hop
- Maximum of 2-hop for performance
Processor Topology is a Ring

- Key to Maximum Performance is traffic balance
- For example, there are 2 shortest routes for traffic between 0 and 7
- Always choose the route least used by previous selections
- Dynamic algorithm gives good result – but can be further tuned

Traffic Balance is a Key to Performance
Route Table Entries - RTA

• Key Feature of Rbox
• Initialized by Firmware
• Route Table Entries (RTA) direct messages
  – From Internal Box to Correct External Port
  – Incoming from one External Port to another External Port (pass-through)
• Each RTA Entry Includes choice of VN0/VN1
  – VN0 and VN1 are alternate transaction trackers
  – Prevent deadlocks that might occur if only VNA was used
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1. Analyze the Technical Challenges

2. Break up development into testable pieces
Steps to be Ready for Power-On

- Project unit-test criteria were created
- 8-Way features were tested on 4-way

<table>
<thead>
<tr>
<th>STAGE</th>
<th>REQUIREMENT</th>
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<tbody>
<tr>
<td>SEC - (pre-PEI CPU Startup)</td>
<td>Expand check-in table</td>
</tr>
<tr>
<td>PEI – QPI Init</td>
<td>Discovery topology, Build Routing,</td>
</tr>
<tr>
<td>PEI – Memory Init</td>
<td>Verify 8-way Compatibility</td>
</tr>
<tr>
<td>DXE – MPCPU Protocol</td>
<td>Expand data tables</td>
</tr>
<tr>
<td>DXE – ACPIPLATFORM</td>
<td>Build expanded ACPI Tables</td>
</tr>
<tr>
<td>SMI – SMI Handler</td>
<td>Expand TSEG allocation</td>
</tr>
<tr>
<td>RAS – RAS Drivers</td>
<td>Identify 8-way impact on RAS</td>
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Supporting 8-way Routing

- 8-socket is not a standard supported feature of Intel® QPI Init Reference Code

Steps of Routing Code
1. SBSP Selected
2. ID neighbors. ID neighbor’s neighbors.
3. Walk all links building node list (tree)
4. Assign Virtual Network VN0, VN1 to links
5. Program RTIDs for directed Messages
6. Program RTIDs for Broadcast
Unit Test the Router

- Insyde needed to write complex code to build 8-way router entries but CRB was only 4-way
- Solution: QPISIM software simulator executes router code on desktop
- Insyde and Inspur engineers studied output and compared against desired
- Simulator can also test routing with non-standard configuration
  1. Fewer than 8 Sockets populated
  2. Intel® QPI Link failures – does the system fallback?
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Conclusions
Smooth Scaling

- Power-on completed ahead of schedule with all sockets working
- Intel® QPI allows system to scale from 2 to 4 to 8 socket while maintaining consistent architectural elements
- UEFI Firmware also scales using:
  - Modularity
  - Defined Interfaces
  - Architected Flow of Control
Next Steps

- Key Understandings:
  - *Intel® QPI Architecture scales smoothly from 1 to 8 Sockets*
  - *UEFI Firmware is mature and ready for the toughest challenges*
  - *For increased schedules confidence break your project into testable pieces*
Additional resources on UEFI:

- Other UEFI Sessions – Next slide
- More web based info:
- UEFI Plugfest Event at Intel in Dupont Washington, June 22-25, 2010 [www.uefi.org](http://www.uefi.org) or email: [laurie.jarlstrom@intel.com](mailto:laurie.jarlstrom@intel.com)
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<td>Using the Latest EFI Development Kit (EDK II) for UEFI Advanced Development</td>
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<td>and Innovation</td>
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<td>Notebook Advancements for Unified Extensible Firmware Interface (UEFI) for</td>
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<td>UEFI Fast Boot for Microsoft* Windows* 7: Fast Boot Without Compromising</td>
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<td>Insyde</td>
<td>your BIOS</td>
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Rev. 1/14/10